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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,222	08/28/2003	Mohit Kapur	YOR920030306US1	6362
7590 Ryan, Mason & Lewis, LLP 90 Forest Avenue Locust Valley, NY 11560			EXAMINER SIDDQUI, SAQIB JAVAID	
			ART UNIT 2138	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE 3 MONTHS			MAIL DATE 03/21/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/650,222

Applicant(s)

KAPUR ET AL.

Examiner

Saqib J. Siddiqui

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/04/06.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


GUY LAMARRE
PRIMARY EXAMINER

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/28/03 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Applicant's response was received and entered December 04, 2006.

- Claims 1-17 are pending.
- Application is currently pending.

Response to Amendment

Applicant's arguments claims 1-17 have been fully considered but they are moot under new grounds of rejection. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the delay element must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first and second paragraph of 35 U.S.C. 112:

- 1) The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 2) The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 6 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Neither the specification, nor the drawings mention any delay element or an apparatus that causes a delay in the signal. The specification is silent on the generation of the delayed signal.

Claims 1, 6, 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not explain how the propagation of the error bit is prohibited. There is mention in paragraph [0030] that the error bit is prohibited to propagate by inversion. However, that is not prohibition that is error correction, which are two different things in the art. Further, with respect to claim 12 the specification does not teach how the input PRBS is related to the output PRBS.

As per claims 2-5, 7-10, 13-17:

These claims are rejected by virtue of their dependency.

Claims 1, 6 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear whether the delayed signal is the same signal as the input signal or is it a new signal. From the claim language it can be interpreted that the two signals are the same with just an added delay and therefore

it is not clear how the error will be detected, as the same signals are being compared with each other.

Claims 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what the relationship is between the input PRBS and the output PRBS. The word "generating" refers to a new signal being generated, therefore if a new signal is being generated in response to the input signal then there is always going to be a mismatch. It is not clear whether the PRBS is being checked for errors or the DUT is being tested if it propagates the PRBS without any manipulation.

Claims 1, 6, 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between the input signal and the output signal. What are they being compared for when they are essentially the same signals.

Claims 1, 6, 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: DUT. From the claim language it may be implied that the DUT is being tested on whether the PRBS passes through it without any propagation errors, and hence the comparison of the same signals is being made. Therefore, there is a need to include the DUT, if that is the claimed inventions.

As per claims 2-5, 7-10, 13-17:

These claims are rejected by virtue of their dependency.

For the purposes of compact prosecution Examiner assumes that Applicant is teaching the self-synchronization techniques as taught in Figure 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2, 4-7, 9-12 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Applicant Admitted Prior Art) and further in view of Schmidt et al. US Patent no. 4,627,057.

As per claims 1 and 11:

AAPA substantially teaches a method and an article of manufacture of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 3) generated by a device in response to an input PRBS received by the device (Figure 1 # 120), the

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method comprising the steps of: delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the output PRBS (Figure 3 # RX1), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 3 # RX1); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

AAPA does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of AAPA, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the error bit from effecting the whole system and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

As per claims 2 and 7:

Schmidt et al./AAPA teaches a method further comprising the step of counting errors (Figure 3 # 332).

As per claim 4:

Schmidt et al./AAPA teaches a method further comprising the step of detecting the non-presence of a PRBS from the device (column 6, lines 4-10).

As per claim 5:

Schmidt et al./AAPA teaches a method wherein the device is one of a communication circuit and a communication channel (Figure 1 #10, "COMPUTER").

As per claim 6:

Schmidt/AAPA teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 10, column 4, lines 29-31), the apparatus comprising: a memory (Figure 1 # 37); and at least one processor coupled to the memory and operative to (Figure 1 # 12): (i) for a given clock cycle (Fig 2, column 4, lines 43-48), detect the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and (ii) prohibit propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

As per claim 9:

Schmidt et al./AAPA teaches an apparatus wherein at least one processor is further operative to detect the non-presence of a PRBS from the device (column 6, lines 4-10).

As per claim 10:

Schmidt et al./AAPA teaches an apparatus wherein the device is one of a communication circuit and a communication channel (Figure 1 #10, "COMPUTER").

As per claim 12:

Schmidt et al./AAPA teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31)

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generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

As per claim 17:

Schmidt/AAPA teaches the apparatus further comprising a third logic detector coupled to the shift register chain for detecting the non-presence of a PRBS from the device (column 6, lines 4-10).

Claim 3 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al./AAPA US Patent no. 4,627,057 and further in view of Gilley US Patent no. 6,215,876 B1.

As per claims 3 & 8:

Schmidt et al./AAPA substantially teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 #

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22, column 4, lines 33-37), the method comprising the steps of: for a given clock cycle (Fig 2, column 4, lines 43-48), detecting the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

Schmidt et al. does not explicitly teach the correction of the error bit.

However, Gilley in an analogous art teaches a method wherein the testing procedure further comprises correcting the error bit (Figure 4 # 78, column 7, lines 1-5). It would have been obvious to one skilled in the art to correct the error bit within the testing device of Schmidt, since one skilled in the art would have realized that correcting the error bit would improve the testing procedure and make it complete. Further it is common knowledge in the art to correct the error once it has been detected.

Claim 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al./AAPA US Patent no. 4,627,057 and further in view of Jungerman US PG Pub No. 20020063553 A1.

As per claim 13-14:

Schmidt et al./AAPA. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for

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detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

Schmidt/AAPA et al. does not explicitly teach the apparatus to allow enough clock cycles for the input PRBS to initialize the shift register chain.

However, Jungerman in an analogous art teaches the apparatus further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain (Figure 2, paragraph [0020]). It would have been obvious to one skilled in the art to initialize the apparatus in Schmidt et al.'s testing procedure since that would account for a predictable test pattern and will also detect any initial flaws in the apparatus.

As per claims 15 & 16:

Schmidt et al./AAPA substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register

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chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

Schmidt et al./AAPA does not explicitly teach the apparatus to allow enough clock cycles for the input PRBS to initialize the shift register chain, an error counter and an error count display.

However, Jungerman in an analogous art teaches the apparatus further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain (Figure 2, paragraph [0020]), an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS (Figure 1 # 124) and an error count display coupled to the error counter for displaying the error count (Figure 1 # 128). It would have been obvious to one skilled in the art to initialize the apparatus in Schmidt et al.'s testing procedure since that would account for a predictable test pattern and will also detect any initial flaws in the apparatus. Also, it would have been obvious to one skilled in the art to use

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the counter element within the testing device of Schmidt, and display the error count since anybody skilled in the art would have realized that using a counter will help keep track of the error rate per clock cycle. Further it is common knowledge in the art to use a counter, during a testing procedure, and display the results of the counter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Saqib Siddiqui
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03/08/2007